ABSTRACT

A method for producing a chip-scale electronic package produced at a substrate level, the substrate including at least one chip having input/output pads on a substrate face. The method a) forms, using a complex mold or stencil, an insulating stress relaxation layer on the front face, the relaxation layer covering the front face of the substrate with a surface relief that provides access wells at input/output pads and protruding parts configured to relax stresses, with each protruding part having a tiered shape including at least one protuberant zone and at least one zone that is recessed in relation to the protuberant zone and is configured to support an electrical bonding pad, b) forms electrically conductive tracks on the relaxation layer to connect input/output pads to the corresponding electrical bonding pads, and c) forms electrical contacts with an exterior on electrical bonding pads.